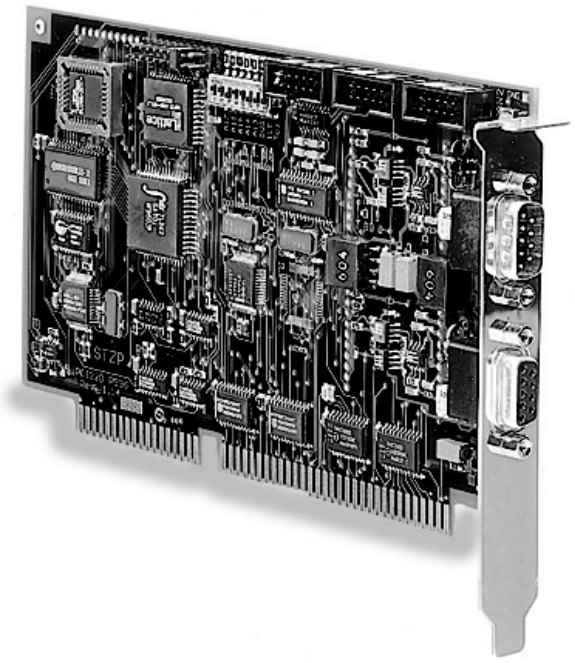
Hardware Manual

iPC-I 320

Intelligent PC/CAN Interface



IXXAT

The expert for industrial and automotive communication

IXXAT

Headquarter
IXXAT Automation GmbH
Leibnizstr. 15
D-88250 Weingarten

Tel.: +49 (0)7 51 / 5 61 46-0
Fax: +49 (0)7 51 / 5 61 46-29
Internet: www.ixxat.de
e-Mail: info@ixxat.de

US Sales Office
IXXAT Inc.
120 Bedford Center Road
USA-Bedford, NH 03110

Phone: +1-603-471-0800
Fax: +1-603-471-0880
Internet: www.ixxat.com
e-Mail: sales@ixxat.com

Support

In case of unsolvable problems with this product or other IXXAT products please contact IXXAT in written form by:

Fax: +49 (0)7 51 / 5 61 46-29
e-Mail: support@ixxat.de

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1 Introduction

1.1 Overview

With the IXXAT PC/CAN interface iPC-I 320 you have purchased a high-quality electronic component which has been developed and manufactured according to the latest technological standards.

The aim of this manual is to help you familiarize yourself with your interface, also referred to in the following as iPC-I 320. Please read this manual before beginning with the installation.

The manual also describes, among other things, the hardware architecture of the interface, knowledge of which is required in order to create your own applications on the interface.

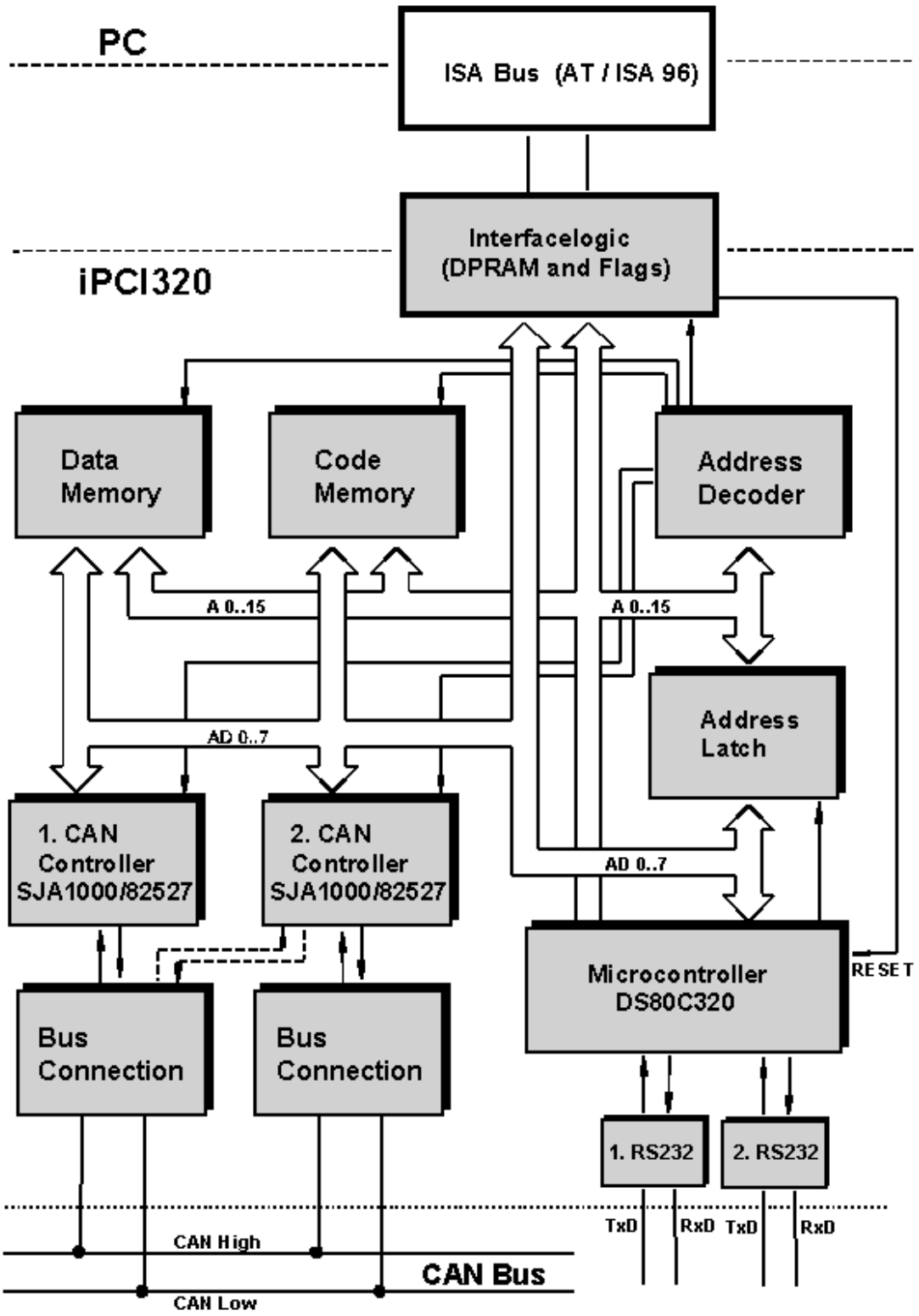
If you are using the interface with the IXXAT VCI driver or other IXXAT software, you can leave out Section 4. For information concerning the development of own software running on the interface, please contact IXXAT or take a look on the support area of the IXXAT homepage.

1.2 Features

The most important technical features are as follows:

- Design as ISA card (PC plug-in card, half length), PC/104 card or AT96 / ISA96 card (Euro card format)
- 8-bit memory-mapped access (7 kbytes address space required)
- Base address can be set in the PC via DIP switch (in the range of C000h-FE00h in 8k steps)
- PC interrupts can be set via jumpers (IRQ 3, 4, 5, 7, 9, 10, 11, 12, 14, 15)
- Microcontroller DALLAS 80C320 with 22.1184 MHz frequency (command compatible with INTEL 8032)
- One or two CAN circuits via Philips SJA1000 and/or INTEL 82527 CAN controller with 16 MHz frequency
- 4 kbyte dual-port RAM (DPRAM), 8 semaphore registers
- 32 kbyte EPROM (optional 64 kbyte EPROM)
- up to 63 kbytes code loadable
- up to 2x56 kbytes XDATA RAM operable
- two serial interfaces according to RS232C as an option
- CAN bus transceivers according to ISO/IS 11898 High Speed are on board (electrically isolated as an option); alternatively, bus couplings can be made via pin boards and plug-in cards
- optionally one or two CAN protective circuits on board
- downloadable (Intel HEX file format); max. 56 kbytes code
- various memory architectures (Harvard, von-Neumann)
- EMC compatible printed circuit design (4-layer multilayer)

1.3 Block diagram



2 Installation

2.1 Hardware installation

For all work on the PC and interface, you must be statically discharged. The work must be carried out on an earthed, anti-static work-mat.

Carry out the following work in sequence:

(1) Establish a free memory segment on the PC of at least 8 kbyte in the range < 1MB (ISA memory range) and a free IRQ. For this, read the manual of your PC.

(2) Set this memory segment and the IRQ on the interface, as described in Section 3.1.

(3) Switch the PC off and remove the mains plug.

(4) Open the PC according to the instructions of the PC-manufacturer and determine a suitable plug-in space.
The interface is designed according to the PC-standard and can be easily built into the computer. Do not use force when plugging in.

(5) Ensure that the interface is held safely in place in the PC.

(6) If your interface is assembled with 2 isolated CAN-circuits, you must fix the additional slot plate and plug in the header on the interface (see Section 3.2).

(7) Close the PC; the hardware installation is now completed.

2.2 Software installation

To operate the interface, a driver is required.
For the installation of the CAN driver VCI under Win95/98/NT/2000, please read the VCI installation manual.

3 Configuration

3.1 Jumper settings

The diagrams Fig. 3-1 (PC/104), Fig. 3-2 (ISA Slot) and Fig. 3-3 (AT/ISA96) show the positions of the plugs and jumpers on the various interfaces.

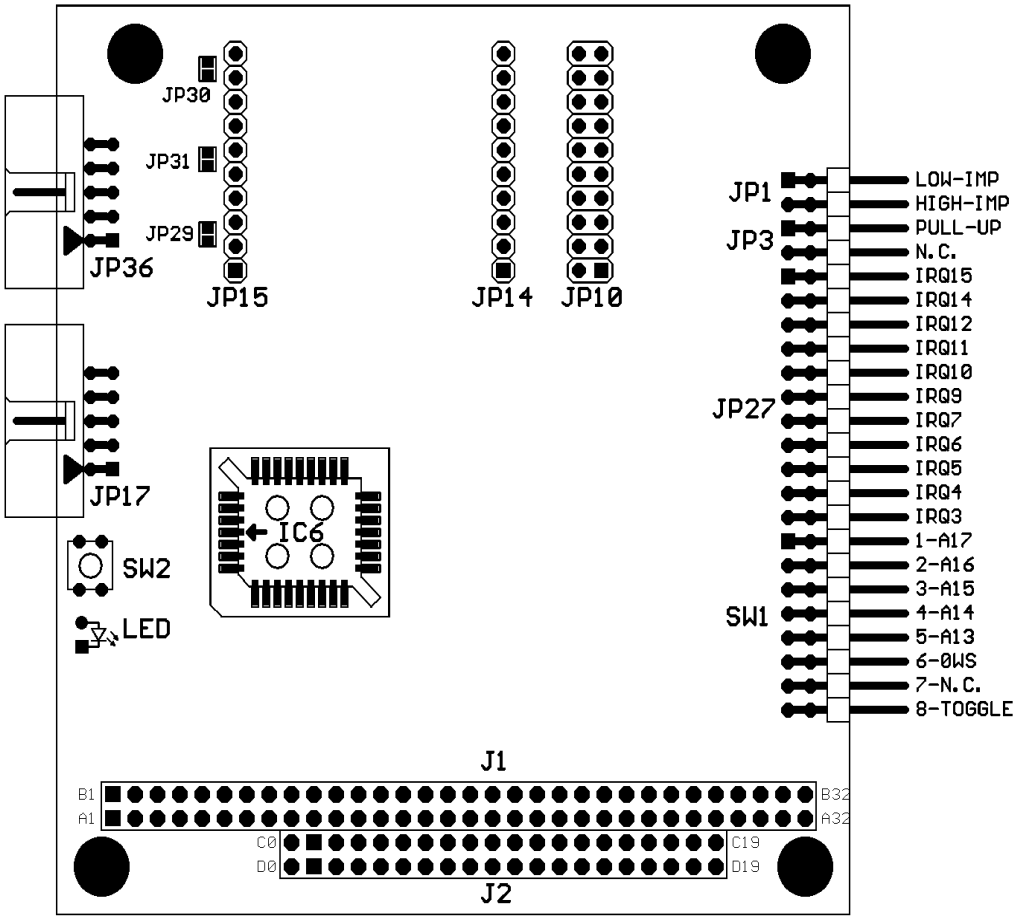


Fig. 3-1: iPC-I 320 PC/104 interface for PC/104 computer

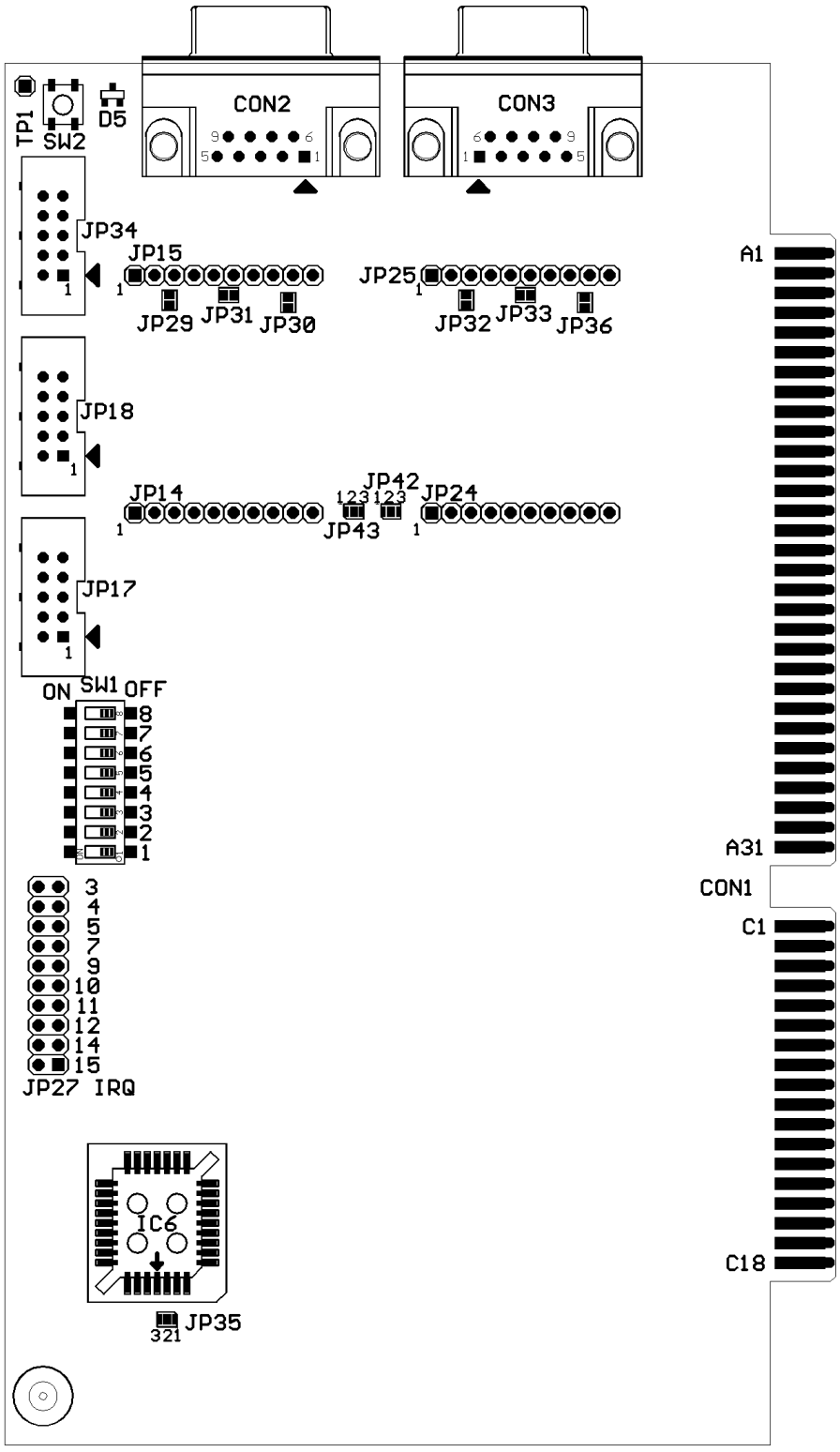


Fig. 3-2: iPC-I 320 interface for ISA slot bus

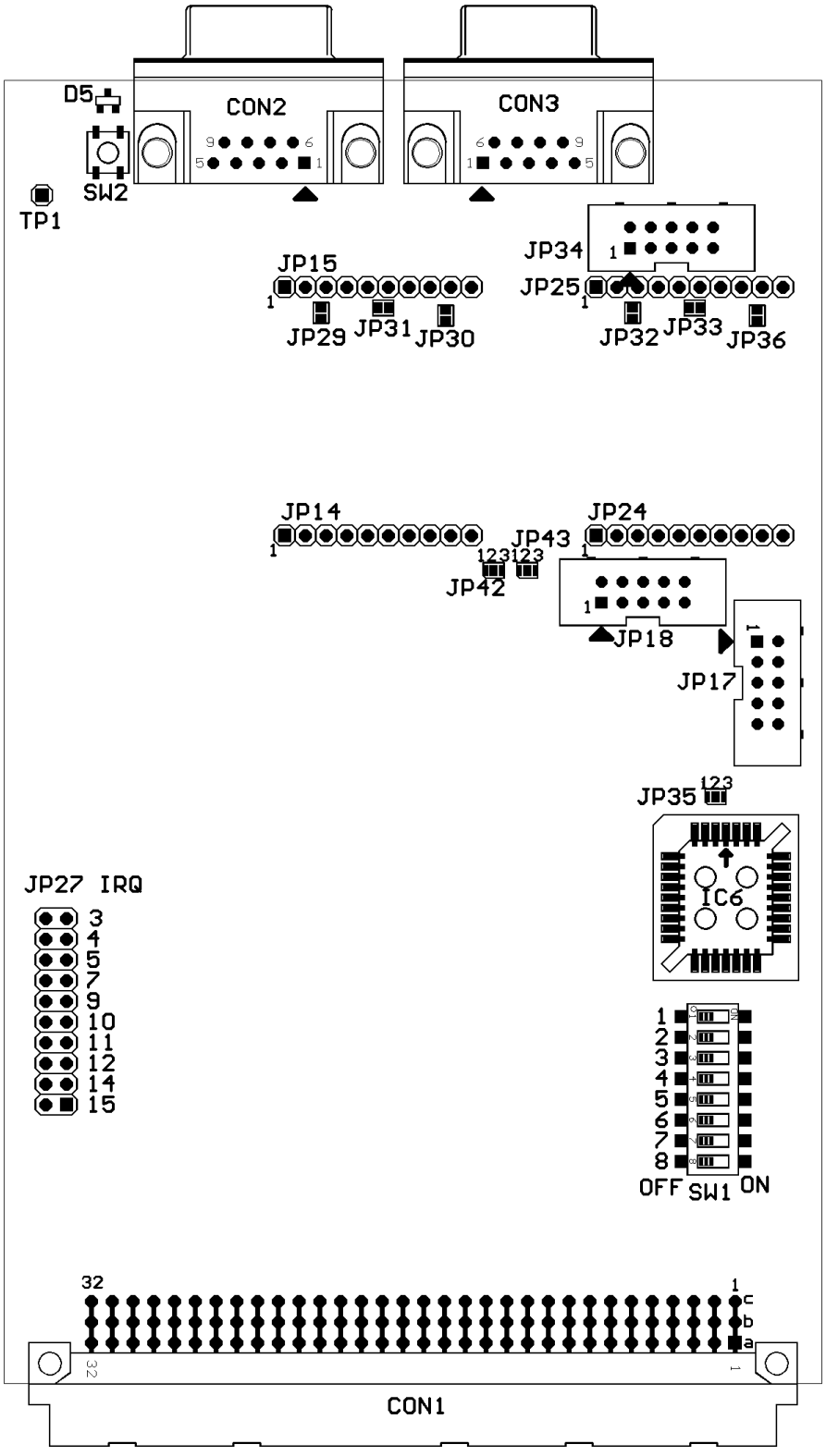


Fig. 3-3: iPC-I 320 AT/ISA96 interface

3.1.1 Setting the base address

For the base address, switches 1 to 5 of the DIP switch SW1 are used (jumper board SW1 with PC/104, ON = jumper plugged in). The following table shows the possible settings (default = factory setting).

Base address	SW1-1	SW1-2	SW1-3	SW1-4	SW1-5
C000h	ON	ON	ON	ON	ON
C200h	ON	ON	ON	ON	OFF
C400h	ON	ON	ON	OFF	ON
C600h	ON	ON	ON	OFF	OFF
C800h	ON	ON	OFF	ON	ON
CA00h	ON	ON	OFF	ON	OFF
CC00h	ON	ON	OFF	OFF	ON
CE00h	ON	ON	OFF	OFF	OFF
D000h (default)	ON	OFF	ON	ON	ON
D200h	ON	OFF	ON	ON	OFF
D400h	ON	OFF	ON	OFF	ON
D600h	ON	OFF	ON	OFF	OFF
D800h	ON	OFF	OFF	ON	ON
DA00h	ON	OFF	OFF	ON	OFF
DC00h	ON	OFF	OFF	OFF	ON
DE00h	ON	OFF	OFF	OFF	OFF
E000h	OFF	ON	ON	ON	ON
E200h	OFF	ON	ON	ON	OFF
E400h	OFF	ON	ON	OFF	ON
E600h	OFF	ON	ON	OFF	OFF
E800h	OFF	ON	OFF	ON	ON
EA00h	OFF	ON	OFF	ON	OFF
EC00h	OFF	ON	OFF	OFF	ON
EE00h	OFF	ON	OFF	OFF	OFF
F000h	OFF	OFF	ON	ON	ON
F200h	OFF	OFF	ON	ON	OFF
F400h	OFF	OFF	ON	OFF	ON
F600h	OFF	OFF	ON	OFF	OFF
F800h	OFF	OFF	OFF	ON	ON
FA00h	OFF	OFF	OFF	ON	OFF
FC00h	OFF	OFF	OFF	OFF	ON
FE00h	OFF	OFF	OFF	OFF	OFF

The address zone of the interface must not overlap with any other system components in the PC.

3.1.2 Setting the PC interrupt

The required PC interrupt is set with the jumper board JP27 by closing the jumper belonging to the required IRQ.

Only <u>one</u> interrupt may be selected for the iPC-I 320!

If no interrupt is required, no pin may be bridged by JP27.

The factory setting of the interface is IRQ 5.

The iPC-I 320 can also be operated with an 8-bit slot. Then interrupts 10-15 are not available.

It should be ensured that no other system component is occupying the selected interrupt, except for cards which work with shared interrupts.

In PC systems it is possible that several cards share an interrupt. Further information on this subject can be found in the hardware manuals for the PC. The iPC-I 320 supports shared interrupts by enabling the level of the interrupt impulses to be adjusted with switch 7 of the DIP switch SW1 (with PC/104 interface via jumper board JP1).

IRQ level	ISA slot, AT/ISA96 SW1-7	PC/104 JP1
Low impulse (default)	OFF	LOW
High impulse	ON	HIGH

For shared interrupts, the switch SW1-7 must be set to OFF, with the PC/104 version the jumper JP1-LOW must be closed.

With the PC/104 interface, both jumpers must never be closed at the same time!

On the iPC-I 320/104 interface it is possible to connect a pull-up resistor with a value of 15 kOhms to the interrupt lead by closing the jumper JP3. When the interface is delivered, the jumper is open.

3.1.3 Selection of the EPROM size

With the ISA and AT/ISA96 versions, there is a PLCC32 socket with EPROM (IC6) on the interface.

The sizes 27C256 (32 kbytes x 8) and 27C512 (64 kbytes x 8) are supported. The EPROM may have an access speed of max. 90 ns. The solder jumper JP35 defines the setting of the EPROM size:

EPROM type	Solder strap on JP35
27C512	1 - 2
27C256	2 - 3

The PC/104 interface has a flash EPROM with 128 kbytes x 8.

3.1.4 Disable toggle

With switch 8 of the DIP switch SW1 (terminal strip SW1 with the PC/104 version, ON = jumper plugged-in), the toggle of the memory architecture can be disabled from the PC. Then the interface always runs in loader-mode after a reset, i.e. the program is always started in the EPROM. In this mode, bank-switching of the XDATA RAM is possible on the interface.

Toggle	SW1-8
possible (default)	OFF
not possible	ON

3.1.5 Setting bus access cycles

With switch 6 of the DIP switch SW1 in ON-position (jumper board SW1 with the PC/104 version, ON = jumper plugged in), the bus can be set with 0 wait states. If SW1-6 is set to OFF, the standard bus cycle is executed.

Bus access	SW1-6
Standard bus access (default)	OFF
0 wait states bus access	ON

3.1.6 Providing current supply via CAN plug

With the solder jumpers JP29, JP30, JP31, JP32, JP33 and JP36, the VCC (5V) or GND signals can be connected to the CAN plug of the two CAN circuits. For this, the jumpers given in the following table have to be closed.

Pin board JP15/JP25 Pin Signal	Default setting	CAN circuit 1	CAN circuit 2
3 - GND	Closed	JP29	JP32
6 - GND	Open	JP31	JP33
9 - VCC	Open	JP30	JP36

Attention: This voltage may be loaded with max. 100 mA.

If the bus transceiver is electrically isolated, GND and VCC are also connected electrically isolated from the interface to the plug board via the solder jumpers.

With the PC/104 version, only the jumpers JP29, JP31 and JP30 are available; they are on the back of the interface.

3.1.7 Reset button and LED

With the order option "developer version", the reset button SW2 and the LED D5 is assembled in addition to the two serial interfaces (with the PC/104 design only one serial interface). The LED is controlled by the microcontroller via port 3.4, whereby the LED is on with a low signal (bit on 0). It is to be observed that the port pin 3.4 is also led out onto the pin boards JP14 and JP24.

3.1.8 Earth connection for measuring purposes

There is a connection on the iPC-I 320 ISA and AT/ISA96 for an earth pin. In Fig. 3-2 and Fig. 3-3 it is marked as TP1 and on the circuit board with the abbreviation GND next to the drill hole.

With the PC/104 version there is no additional earth connection.

3.1.9 Jumper for port pins 1.2 and 1.3

With the solder jumpers JP42 and JP43, the port pins 1.2 and 1.3 are either connected to a serial interface chip (if available) or to the pin boards JP14 and JP24. If no RS232 chip (developer version) is assembled, JP42 and JP43 are open. These two jumpers are not available in the PC/104 version.

Jumper	Position1-2*	Position 2-3
JP42 (P1.2)	P1.2 on RS232 chip	JP1.2 on JP14 and JP24
JP43 (P1.3)	P1.3 on RS232 chip	JP1.3 on JP14 and JP24

* 1-2 bridged, default setting with assembled RS232 interface

3.2 Design of the CAN plugs

One (common) or two isolated high-speed bus transceivers according to ISO/IS 11898 may be present on the interface. The signals of the first bus transceiver connect with the 9-pin sub-D-pin/bush CON2/3. With the PC/104 version the signals are available via the pin board JP36. If two isolated bus transceivers are assembled, the signals for the CAN bus of the second bus transceiver connect with the header JP34. With the PC/104 version a second CAN circuit is available as plug-in circuit board. Both bus transceivers can be electrically isolated from the CAN bus as an option.

A version without bus transceiver is available on the interface as a further option. In this case the signals are led out onto two pin boards each (JP14/JP15 for the first CAN circuit, JP24/JP25 for second CAN circuit). This enables alternative bus transceivers to be implemented.

A CAN protective circuit, consisting of a special CAN coil is also available as an option. The circuit suppresses faults and short spikes on the CAN lines.

3.3 Pin assignment

The following plugs are on the interface:

Plug	ISA slot	PC/104	AT/ISA96
CAN1	CON2, CON3 JP14, JP15	JP36 JP14, JP15	CON2, CON3 JP14, JP15
CAN2 (isolated from CAN1)	JP34 or JP24, JP25	-	JP34 or JP24, JP25
1. RS232 interface (optional)	JP17	JP17	JP17
2. RS232 interface (optional)	JP18	-	JP18
PC bus	CON1	J1 + J2	CON1

3.3.1 Connection between CAN controllers and bus transceivers

The signals of the CAN controllers 1/2 and up to four port pins of the microcontroller connect with JP14/JP24.

Pin no. JP14/JP24	Signal
1	VCC
2	GND
3	Port 1.3*
4	RX0
5	RX1
6	TX1
7	TX0
8	Port 3.4
9	Port 1.2*
10	Port 3.5

* Adjustment via JP42 and JP43 as described in 3.1.9

JP15 leads the signals of the **first bus transceiver** to the 9-pin CON2 plug (male) and the 9-pin plug (female) CON3 (at the PC/104 version to JP36).

Pin no. JP15	Pin no. CON2/CON3	Signal name
1	1	
2	2	CAN Low
3	3	GND (via JP29)
4	4	
5	5	
6	6	GND (via JP31)
7	7	CAN High
8	8	
9	9	VCC (via JP30)
10	-	

With electrically isolated bus transceivers the signals GND and VCC are also electrically isolated from the GND and VCC signals of the interface.

JP25 leads the signals of the **second bus transceiver** to the 10-pin header JP34.

Pin no. JP25	Pin no. JP34	Signal
1	1	
2	3	CAN Low
3	5	GND (via JP32)
4	7	
5	9	
6	2	GND (via JP33)
7	4	CAN High
8	6	
9	8	VCC (via JP36)
10	10	

With electrically isolated bus transceivers the signals GND and VCC are also electrically isolated from the GND and VCC signals of the interface.

If the CAN protective circuit is assembled on the circuit board, the signals CAN-Low and CAN-High are connected from JP15 (JP25) via the protective circuit with CON2/3 (JP34).

3.3.2 Serial RS232 interface

The serial interface can be optional assembled. The signals of the first RS232 interface connect with JP17, the signals of the second RS232 interface with JP18. With the PC/104 version, only the first serial interface is supported.

Pin no. JP17/JP18	Signal	Sub D9 pin
1		
2		
3	RxD	2
4		
5	TxD	3
6		
7		
8		
9	GND	5
10		

4 Architecture

4.1 PC side memory assignment

Communication with the PC is made via a 7 kbyte memory zone in which the 4 kbyte DPRAM, eight semaphore registers and 2 flags (Reset and μC-interrupt) are placed.

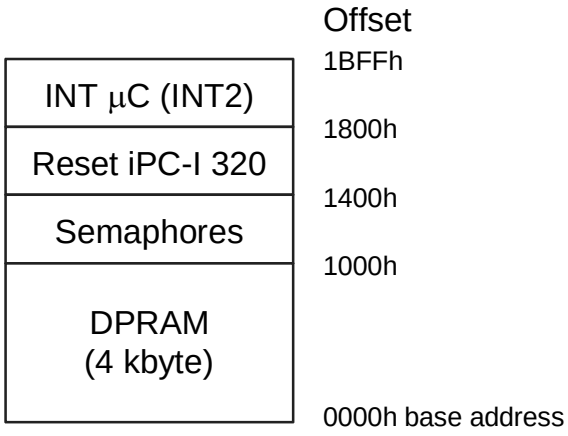


Fig. 4-1: PC side memory assignment

4.1.1 DPRAM

Generally the DPRAM can be accessed from both sides simultaneously. However, this only applies if it is not the same address. In this case differentiation is made between the types of access. Reading from both sides is unproblematic here. However, if writing occurs from one side and reading from the other, the reading side receives either the old data or the data just written. If writing occurs simultaneously from both sides onto the same memory cell, an access conflict occurs. Using so-called semaphores can prevent this collision.

4.1.2 Semaphores

Semaphores, also referred to in this context as semaphore registers, are special memory cells in the DPRAM. They are in a zone which is isolated from the actual DPRAM.

The DPRAM used has eight of such semaphore registers. For their selection, only the three lower value address lines are important, i.e. the eight registers are reflected just as frequently in the range from 1000h to 13FFh (PC side) or from F000h to F3FFh (μC side).

For more information on DPRAM and its semaphore registers, please see the data sheet of the IDT 71342 (addresses in Appendix C).

4.1.3 Reset of the µC from the PC

By writing a defined value (reset value) in a random address of the memory range from 1400h to 17FFh, a reset of the microcontroller is triggered on the interface. The value written in the memory cell states in which memory architecture the interface should be switched after the reset. If the DIP switch 8 (SW1-8) is set to ON, there is no toggle of the memory architecture. The interface then always remains in the loader mode and executes the program contained in the EPROM. The following table shows the reset bit patterns for the toggle. X means irrelevant:

Mode	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Loader/application	X	X	X	X	X	X	X	0
Harvard	X	X	X	X	X	X	0	1
von-Neumann	X	X	X	X	X	X	1	1

4.1.4 Triggering the interrupt on the µC through the PC

By writing a random value in a memory address in the range from 1800H to 1BFFh, an interrupt is triggered on the input INT2 of the microcontroller.

4.2 µC-side memory assignment

The interface can be operated in 3 different memory modes:

- Loader/application-mode (EPROM as code memory, RAM as data memory)
- Von-Neumann-mode (common code and data memory in the RAM)
- Harvard-mode (separate code and data memory in the RAM)

After switching on, the interface is always in the loader-mode. In this mode the program contained in the EPROM on the interface is executed.

4.2.1 Program memory

The program code for the interface can either be loaded into the RAM or directly executed from the EPROM (depending on the memory mode selected). The size of the code memory depends on the selected memory mode:

- Loader/application-mode: 32 kbytes or 63.75 kbytes EPROM as code memory
- Von-Neumann-mode: 63 kbytes plus 256 bytes common code and data memory
- Harvard-mode: 63 kbytes code memory 256 bytes common code and data memory

4.2.2 Data memory

The size of the data memory also depends on the mode selected:

- Loader/application-mode: 63 kbytes data memory for loadable program (SW1-8 OFF) becomes the code memory in Von-Neumann and Harvard mode, 2x56 kbytes data memory (bank-switching, SW1-8 ON)
- Von-Neumann mode: 56 kbytes plus 256 bytes common memory for code and data
- Harvard mode: 56 kbytes data memory plus 256 bytes common code and data memory

4.2.3 Loader/application mode

In the loader/application mode, 32 kbytes and 63.75 kbytes EPROM respectively are available for the program code. In the EPROM memory, a loader or an application can be firmly implemented.

As shown in Fig. 4-2 and Fig. 4-3, 56 kbytes of memory are available in the XDATA area of the controller, in which the application data can be filed. If the interface is operated in "Disabled toggle" mode (see 3.1.4), the RAM-BANK 1 in the XDATA area can be displayed by writing a random value in the address range between FC00h and FCFFh, the RAM-BANK 0 by writing between FD00h and FDFFh.

Access to the DPRAM, the semaphores and the CAN-controllers (only with SW1-8 ON) also occurs via XDATA address areas.

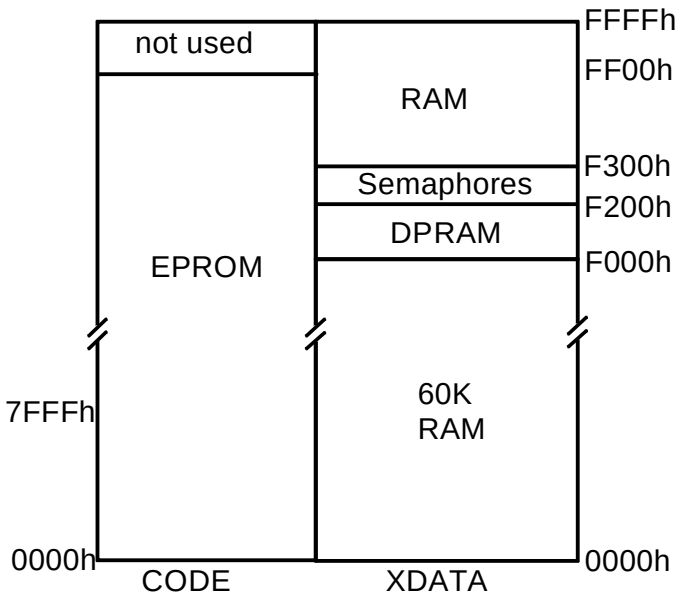


Fig. 4-2: Storage assignment in loader-mode (DIP SW1-8 OFF)

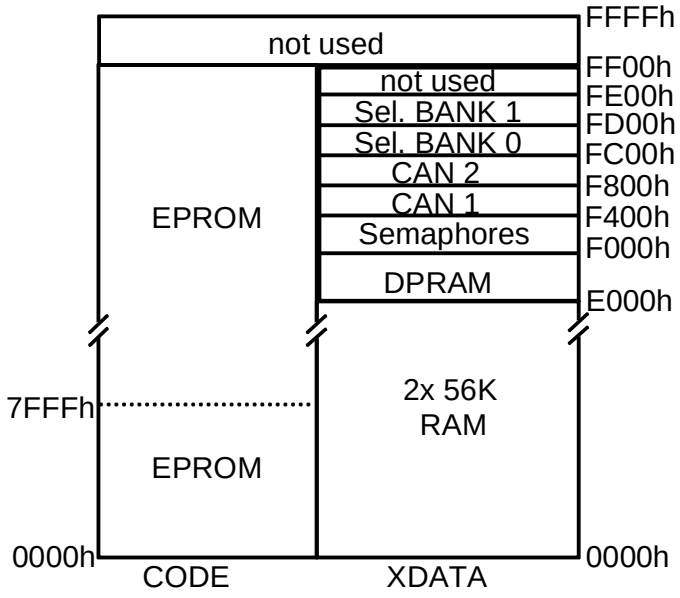


Fig. 4-3: Storage assignment in application-mode (DIP SW1-8 ON)

4.2.4 Harvard-mode

In Harvard-mode the programmer has the largest possible memory pool available (see Fig. 4-4). Programs which are loaded via the loader into the code area can contain a maximum of 63.25 kbytes code. 0.75 kbytes (from F000h to F2FFh) of the available address space must remain unused, since in loader-mode, because of the DPRAM displayed here as well as the semaphores, it is not possible to write in this area.

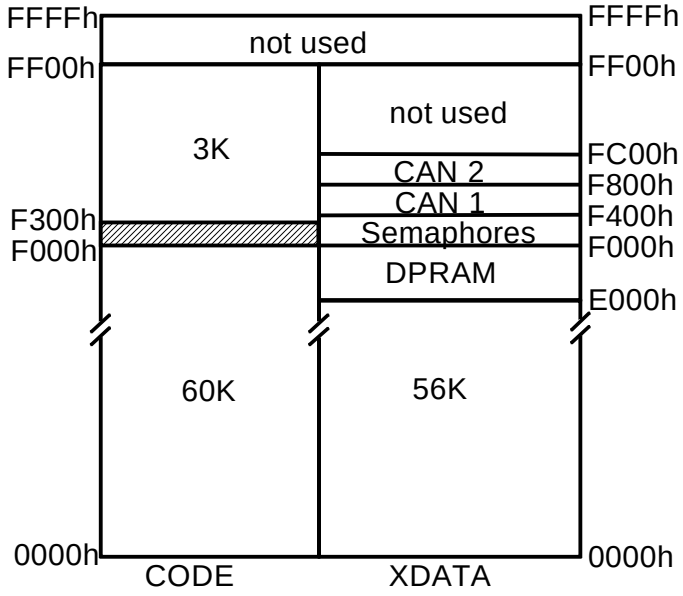


Fig. 4-4: Storage assignment in Harvard-mode

4.2.5 Von-Neumann mode

The Von-Neumann mode provides applications with the smallest usable storage area (see Fig. 4-5). The advantage of this mode is that debuggers such as Keil TS51 can also be implemented, as the whole usable code area can be modified by the software itself.

In the area of the CAN controller, of the DPRAM and of the semaphore register, the storage is decoded as Harvard-storage when accessed.

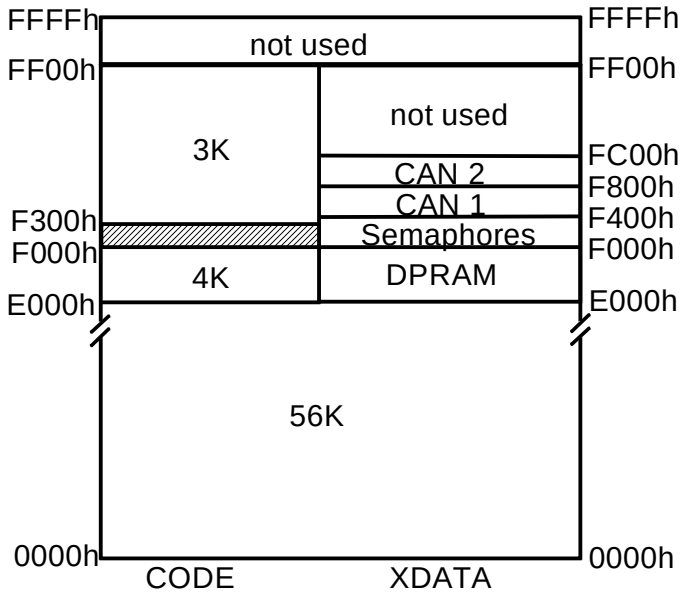


Fig. 4-5: Storage assignment in Von-Neumann mode

4.3 Triggering an interrupt on the PC

The microcontrollers can trigger an interrupt on the PC by writing a low impulse of min. 50ns length onto the port pin 1.7. The electronics on the interface convert this into an impulse of approx. 1.5 μs length (triggering occurs on the falling side of the impulse of the port pin). The requested interrupt on the PC side is set with the jumper JP27, the level of the impulse with switch 7 of the DIP switch SW1 (see Section 4.1.2).

4.4 CAN controllers

Up to two CAN controllers can be present on the interface. These can be controllers of the types Philips SJA1000 or INTEL 82527. With the PC/104 version, the first CAN controller is always a Philips SJA1000, the second CAN controller can be assembled via an optional plug-in circuit board.

The first CAN controller is displayed in the range from F400h to F7FFh, the second CAN controller in the range from F800h to FBFFh in the XDATA area of the microcontroller. When the individual storage area is accessed, the corresponding CAN controller is automatically selected. The exact registration description can be found in the relevant data books of INTEL or Philips (web-addresses in Appendix C). Both CAN controllers have a frequency of 16 MHz.

CAN controller	Start address	INT on DS80C320	HW reset with port	TX0 disable with port
1. CAN controller	F400h	INT0	P1.0	P1.5
2. CAN controller	F800h	INT1	P1.1	P1.6

The CAN controllers are reset by a high-level (bit on 1) of the port bits to P1.0 and P1.1 respectively. After reset of the microcontroller, it should be ensured that the two CAN controllers are in reset mode. The application on the interface must ensure that the two port bits are set to 0.

It is possible, with a high level (bit on 1) of the port bits 1.5 and 1.6, to prevent the INTEL 82527 CAN controller from transmitting. For this, the TX0 line of the CAN controller to the bus coupling is interrupted. After a reset of the microcontroller, it is the task of the application to set the bit to 0, in order to enable transmission.

It should be ensured that the Output Control Register of the Philips SJA1000 CAN controller is loaded with the value 5Eh. To ensure correct functioning of the INTEL 82527 CAN controller, the value 41h must be written in the CPU interface register of the INTEL 82527 after each reset of the CAN controller.

Since the INTEL 82527 CAN controller has a relatively slow CPU interface, it is necessary to insert wait states when accessing the CAN controller. The DALLAS DS80C320 microcontroller has the CKCON register (SFR Register 8Eh) for this purpose. The value 100b must be entered in bits 2, 1 and 0 of the CKCON register (corresponds to 6 wait states when accessing the XDATA area). Depending on the application, it is helpful to set the wait states only when accessing the CAN controller. If parts of a program is only working with data from the RAM, the wait states should be cancelled.

For the Philips SJA1000, 4 wait states (010b) are sufficient.

4.5 Serial interfaces

Up to two serial interfaces according to RS232C standard can be assembled on the card. The interfaces are operated by the microcontroller via the integrated serial interfaces of the DS80C320 on the port pins P3.0/P3.1 and P1.2/P1.3.

Appendix

Appendix A

Technical data

The following data refer to the basic version of the interface (one Philips SJA1000 CAN controller, one bus transceiver according to ISO/IS 11898, loader EPROM 27C256)

Dimensions:

- ISA slot version: 107 x 178 mm (without slot plate)
  127 x 193 mm (total)
  22 mm overall height
  Weight: approx. 120g
- PC/104 version: approx. 101 x 96 mm
  23 mm overall height
  Weight: approx. 60g
- AT/ISA96 version: 100 x 167 mm (Europa card)
  12 mm overall height
  Weight: approx. 120g

Working temp. range:	0 - 50°C
Power supply:	5V DC ± 5%
Current consumption:	typically 190 mA
	max. 600 mA
EMC test according to:	EN 50081-1:1992
	EN 50082-2:1994

Notes on EMC

The PC/CAN interface iPC-I 320 may only be installed in a PC which carries the CE-mark and is fitted with an RF-shielded housing. All cables connected to the interface must have shielded braiding which lies flat on the plug housing. The plug housing must be RF-shielded and have low inductive contact with the PC housing. All unused connections of the PC/CAN interface iPC-I 320 must be closed with RF-shielded covers.

Appendix B

Factory settings

The factory settings of the interface are given in the following table. For special versions of the interface, individual settings may differ.

Base address:	D000h	DIP	SW1-1	ON
		DIP	SW1-2	OFF
		DIP	SW1-3	ON
		DIP	SW1-4	ON
		DIP	SW1-5	ON
PC-interrupt:	IRQ5	JP27 IRQ 5 bridged		
EPROM size:	27C256 (32kBx8)	JP35 2-3 bridged		
Bus wait states:	with wait sates	DIP	SW1-6	OFF
IRQ level:	low impulse	DIP	SW1-7	OFF
Toggle:	possible	DIP	SW1-8	OFF
P1.2 and P1.3:				
- RS232 assembled:	on RS232 module	JP42 1-2 bridged		
(developer option)		JP43 1-2 bridged		
- Without RS232:	no connection	JP42 open JP43 open		

Appendix C

Supply sources for data sheets

Dual-port-RAM IDT 71342LA:
http://www.idt.com

CAN controller Philips SJA1000:
http://www.philips-semiconductors.com

CAN controller Intel 82527:
http:/www.intel.com

Microcontroller Dallas 80C320
http://www.dalsemi.com

EC Declaration of Conformity

IXXAT Automation hereby declares
that the product: iPC-I 320

with the article numbers: 1.01.0040.10100
1.01.0040.10200
1.01.0040.11110
1.01.0040.11220

complies with the requirements of the standards:

EN 55022:87/ Class B
EN 55082-2: 94
EN 61000-4-2:95
ENV 50140:95
EN 61000-4-4:95

In accordance with the following test report: SZ186_01.DOC

The product thus complies with the EC directives: 89/336/EEC

This declaration applies to all devices bearing the CE symbol and loses its validity if modifications are made to the product.

30.06.1998, Dipl.-Ing. Christian Schlegel , Managing Director

IXXAT Automation GmbH
Leibnizstrasse 15
88250 Weingarten