

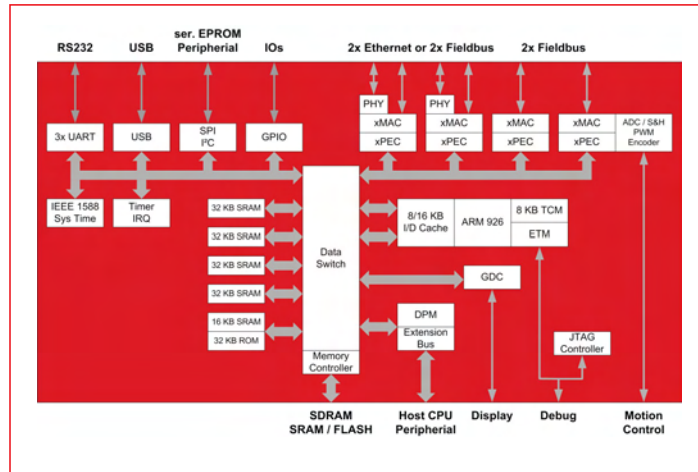
netX 100/500 – networX on chip

The future of communication

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netx

Description

- Flexible “high end” network controller or highly integrated single chip solution for applications and communication
- Four communication channels as Real-Time Ethernet or fieldbus interface individually configurable
- New system architecture optimized for communication and high data throughput
- 32-Bit/200MHz CPU ARM 926 with 200 MIPs computing power for Windows CE and Linux
- Dual-port-memory, AD converter and graphic controller on chip



The netX is a highly integrated network controller with a new system architecture optimized for communication and maximum data throughput.

Based on the 32-Bit CPU ARM 926EJ-S cycled at 200 MHz, it possesses a memory management unit, caches, DSP and Java extensions. The internal memory of 144 KByte RAM and 32 KByte ROM that contains the Bootloader is sufficient for smaller applications whereas for Windows CE and Linux it is supplemented with the 32 Bit Memory Controller memory externally with SDRAM, SRAM or FLASH. The connection to a primary Host is carried out via the Dual-port-memory interface, which is configurable for stand-alone applications also as a 16 Bit extension bus. Comprehensive peripheral functions, serial interfaces such as UART, USB, SPI, I²C as well as the integrated graphic controller permit a wide spectrum of applications. Yet, it is the central data switch and the four freely configurable communication channels with their own intelligence that is the main characteristic of the netX as a “high end” network controller.

The data switch connects via five data paths to the ARM CPU and the communication, graphic and Host controllers with the memory or the peripheral units.

In this way the controllers transmit their data in parallel, contrary to the traditional sequential architecture with only one common data bus and additional bus allocation cycles.

The controllers of the four communication channels are structured on two levels and are identical to each other. They consist of dedicated ALUs and special logic units that receive their protocol functions via Microcode. Two channels possess an additional integrated PHY for Ethernet.

The Medium-Access-Controller xMAC sends or receives the data according to the respective bus access process and encrypts or converts these into Byte depictions.

The Protocol Execution Controller xPEC compiles these into data packets and controls the telegram traffic. These are exchanged in DMA blocks over the memory of the ARM. In addition, every channel has a Dual-port-memory available for status information or as local data picture.

With the intelligent communication ALUs, the netX carries out the most varied protocols and protocol combinations and can synchronize them independently of the reaction time of the CPU – an absolutely new feature in industrial communication technology.



Supported
Real-Time-Ethernet-Systems



Supported
Fieldbus-Systems



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Technical Data

		netX 100	netX 500
Core			
Processor	ARM 926EJ-S, 200 MIPS, ARMv5TE-command set with DSP- and Java-extension	X	X
Cache	16 KByte commands / 8 KByte Data	X	X
Tightly coupled memory	8 KByte Data	X	X
Memory Managment Unit	Windows CE- and Linux-Support	X	X
Internal Memory			
RAM	144 KByte, of this 16 KByte with external voltage supply	X	X
ROM	32 KByte with Bootloader	X	X
Ethernet-Interface			
Ports	2 x 10BASE-T/100BASE-TX, Half-/Full-Duplex, IEEE 1588 time stamp	X	X
PHY	Integrated, Auto-Negotiation, Auto-Crossover	X	X
Real-Time-Ethernet	EtherCAT with three FMMUs and four Sync-Manager	X	X
	Ethernet/IP	X	X
	Modbus IDA		
	Powerlink with integrated Hub	X	X
	PROFINET RT and IRT with integrated Switch	X	X
	SERCOS-III	X	X
Fieldbus-Interface			
If Ethernet is not used, then two additional fieldbusses are available			
	The systems can be combined as desired.	Quantity	1
Fieldbus	AS-Interface, Master only	X	X
	CANopen / DeviceNet, Master and Slave	X	X
	CC-Link, Slave only	X	X
	PROFIBUS, Master and Slave	X	X
Periphery			
Color-LCD-Controller	For TFT-panels, Color-STN- and Mono-STN-panels Resolution 320 x 200 to 640 x 480, color depth 1, 2, 4, 8, 16-Bit		X
Real-Time clock	With external voltage supply		X
IEEE 1588 System Time	32-Bit second counter, 32-Bit Nano second counter	X	X
USB	Revision 1.1, 12 MBaud Full-Speed, Host- or Device-Mode	X	X
UART	16550 compatible, max. 3 MBaud, RTS/CTS support	Quantity	3
I ² C		X	X
SPI	Master- and Slave-Mode, max. 10 MHz, 3 Chip-Select-Signals	X	X
AD-Converter	2 x 4 Channels with 1MS/s Sample&Hold and 10 Bit-resolution Single ended, Common Analog Ground, external reference voltage	X	X
PWM	0–20 kHz/12-Bit-resolution 0–80 kHz/10-Bit-resolution	X	X
Encoder	2 Channels, Impuls quadruplication, digital input filter	X	X
General I/Os	3.3 V/6 mA	Quantity	16
Status LEDs	2 LEDs two-colors, 3.3 V/9 mA	X	X
Memory-Interface			
Memory bus	32-Bit-Databus / 24-Bit-Address bus	X	X
Address region	256 MByte SDRAM / 64 MByte Flash	X	X
Memory modules	SDRAM, SRAM, Flash	X	X
Host-Interface			
Dual-port-memory-mode	8/16-Bit-Databus, 64 KByte configurable in 8 Blocks; emulated by internal RAM	X	X
Extension-Mode	8/16-Bit-Databus, 24-Bit-Address bus, Bustiming adjustable	X	X
PIO-Mode	Freely programmable Inputs and Outputs	Quantity	53
Debug-Interface			
JTAG	ARM-Processor and Boundary-Scan	X	X
ETM	Embedded Trace Macrocell, ETM9 V2 Medium Size	X	X
Operating conditons / housings / various data			
System cycles	200 MHz ARM / 100 MHz Periphery		
Signal level	3.3 V		
Power supply	1.5 V for Core 3.3 V for Input/Output		
Operating temperature	without heat sink with heat sink 10°/W	-40..+70 °C -40..+85 °C	-40..+70 °C -40..+85 °C
Storage temperature		-65..+150 °C	-65..+150 °C
Power consumption	PHYs switched off PHYs switched on	typ. 1.0 W typ. 1.5 W	1.0 W 1.5 W
Housing	PBGA, 1 mm raster	Pins	345
	Dimensions	mm	22 x 22

Note: All technical data can be altered without notice.

Product Overview

Article designation	Article number	Article	Note
netX 100	2220.000	netX 100	Note
netX 500	2220.000	netX 500	

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