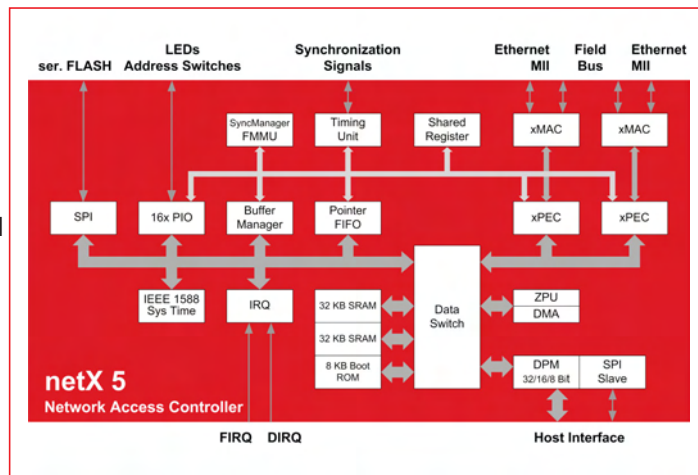


netX 5 – networX on chip Network Access Controller

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netx

Description

- Flexible Network Access Controller
- Two communication channels configurable between Real-Time Ethernet and fieldbus
- Two MII Ports with IEEE 1588 for EtherCAT with 8x Sync / FMMU Powerlink with integrated hub PROFINET IRT with 2-Port switch SERCOS III and others
- Fieldbus controller for AS-Interface CANopen and DeviceNet CC-Link CC-Link PROFIBUS
- 8/16/32 Bit Dual-Port-Memory or serial SPI Host interface



The netX 5 is a highly integrated Network Access Controller with new, flexible, system architecture. It belongs to the family of netX network controllers, but does not possess its own ARM CPU.

With its integrated Dual-Port-Memory or the serial SPI interface, it operates as a companion chip to a Host CPU and makes available the whole spectrum of industrial communication from fieldbus up to the various Real-Time-Ethernet systems. External PHYs must be connected to the two MII interface for Ethernet purposes.

Both transmission channels are used for Real-Time Ethernet, whereas these can be combined as required when configuring as fieldbus controllers. Also of interest is a common controller for Ethernet/IP and DeviceNet, which, with the integrated IEEE 1588 unit, also supports CIP Sync.

The areas of application are communication interfaces in which the Host processor has sufficient computing power to process the whole transmission protocol.

The communication channels are designed to be compatible with the other controllers of the netX family.

They consist of dedicated ALUs and special logic units, which are allocated by their respective protocol functions by means of microcode.

The xMAC Medium-Access-Controller transmits or receives data in accordance with the respective bus access procedures and codes or converts these into a Byte depiction.

The xPEC Protocol Execution Controller combines these into data packets and controls the telegram traffic. Large data quantities are transmitted per DMA blocks into, or out of, the integrated buffer memory whilst a Dual-Port-Memory is available for each channel for status information. Alternatively a Triple-Buffer logic is implemented, which always provides the address of the next free buffer for purposes of conflict-free data exchange.

With the intelligent communication ALUs, the netX processes the most varied protocols and protocol combinations in a single chip – an absolutely new feature in industrial communication technology.



Supported
Real-Time-Ethernet-Systems



Supported
Fieldbus-Systems



netX 5 – details

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Technical Data

Internal Memory			
RAM	64 KByte		
Ethernet-Interface			
Ports	2x MII, 25 MHz PHY Clock output, IEEE 1588 time stamp		
Real-Time-Ethernet	EtherCAT with eight FMMUs and eight Sync-Managers Ethernet/IP Modbus IDA Powerlink with integrated Hub PROFINET RT and IRT with integrated Switch SERCOS-III		
Synchronisation signae	Trigger		
	Sample		
Fieldbus-Interface			
	In place of Ethernet, each channel can be configured as a fieldbus controller		
Fieldbus	The systems can be combined as desired. AS-interface, Master only CANopen, Master and Slave CC-Link, only Slave DeviceNet, Master and Slave PROFIBUS, Master and Slave		
Host-Interface			
Dual-Port-Memory	8 / 16 / 32-Bit-Databus, configurable, emulated by internal RAM		
SPI	Slave-Mode, max. 50 MHz		
Periphery			
IEEE 1588 System Time	32-Bit second counter, 32-Bit Nanosecond counter		
SPI	Master-Mode, max 50 MHz Slave-Mode, max. 33 MHz		
JTAG			
General I/Os	3.3 V / 6 mA	Quantity	16
Operating conditions / Housing / various data			
System cycles	100 MHz		
Signal level		V	3.3 V
Spower supply	for Core	V	1.8 V
	for In/Output	V	3.3 V
Temperature	Operation	°C	-40..+85
	Storage	°C	-65..+150
power consumption		W	tdb
Housing	LFBGA, 0,8 mm raster	Pins	201
	Dimensions	mm	13 x 13

Note: All technical Data are temporary and can be changed without further notice.

Product Overview

Article description	Article No	Article
netX 5	2240.000	netX 5 Network Access Controller

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